Fermi National Accelerator Laboratory

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Engineering Note

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Project: D0 Tracking Electronics
Doc. No: U020207A Rev. A

Subject: Stand-Alone Sequencer Test Procedure

1) Visual inspection
- Are the correct chips installed properly?
- Any obvious soldering problems.
- Ohm meter: 97 ohms +5V to GND

2) Install board into crate. Plug in Altera Byteblaster and program EPLDs on board using MaxPlusII software, Programmer. (Restore jcf from e:\utes\sas2002).
3) Power up SVX AVDD, AVDD2, DVDD, (or SVX Emulator), and observe front panel display 7C1.
4) Use spreadsheet c:\xls32\saseq.xls or d:\xls32\saseqdfnl4.xls. Refer to the description for this board if necessary. Location is at http://d0server1/users/utes/webpage/svxfiles/SA_SEQ.pdf.
5) On SASeq, hit "Download Sequencer". This checks that the first six reads match the first six writes. If SVX is on "A" side of Interface Board, make sure 20 is written to 50D012, if "B" side, set it to 10. This ignores absent HDIs.
6) On "Init SVX", download SVX, make sure # of chips in chain 1,2 is correct. Observe no errors and DTACK LED.
7) On Cal Inject page, do a Cal Inject, make sure PAR and SYNC LEDs don't blink. CAL and DIG lights should blink, and data should be graphed:
- Is Sequencer ID correct
- Is Sequencer Status byte correct
- Are chip Ids correct
- Do channel Ids increment by one
- Is data pedestal within +/- 10 counts
- Is the trailer C0C0 at the end of the data for each used string

8) On Trigger page hit Execute twice, Second one should give data on plot.
9) Repeat steps 3-8 with other half of board.
10) Check SYNC TRIG and BUSY lemos while sending Execute.
11) Check VETO, R_PRE, and CLOCK lemos.
12) Set the Cal Voltage parameter to various values and check that the value read out in the data is within limits. Suggested Cal Voltage values: 00, 01, 02, 04, 08, 10, 20, 40, 80, FF. An alternative is to probe the Vcal pin going to the HDI. Nominal values exist for various values of this parameter in the appendix at: http://d0server1/users/utes/webpage/svxfiles/SA_SEQ.pdf.

13) With a scope probe on the SVX clock line, check crossing pulse width while in Acquire mode. Nominal values exist for various values of this parameter in the appendix at: http://d0server1/users/utes/webpage/svxfiles/SA_SEQ.pdf.
14) Check readout at various pipelines 00, 01, 02, 04, 08, 10, 1F, by setting the Cal Pipe parameter to match the setting of the SVX pipeline depth for one chip. Then make sure the Cal pulses exist in every case using a logic analyzer.
15) Set Sequencer ID to 00, 01, 02, 04, 08, 10, 20, 40, 80, FF and check that the readout header matches.
16) Test the Logic analyzer feature using the Cal and Readout trigger options.
17) Try software reset, bit 7 of CSR1.
18) Check Snapshot Register, 50D014. The eight LSBs should match the front panel hex display.
19) Check FIFO Test Register, 50D016.
20) Using a 40MHz crystal, run cal_inject cycles using slow readout for each half of board.